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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,872	DELANO, ERIC	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been considered. Claims 11 and 17 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 04 April 2005 and Extension of Time Two Months as received on 04 April 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being taught by Batten et al., U.S. Patent Number 6,269,439 (herein referred to as Batten).

5. Referring to claim 1, Batten has taught a method for processing bundled instructions through execution units of a processor, comprising the steps of:

a. Fetching a first bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the first bundle to a first cluster of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

c. Fetching a second bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

d. Distributing the second bundle to a second cluster of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

6. Referring to claim 2, Batten has taught processing the first bundle within the first cluster (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

7. Referring to claim 3, Batten has taught processing the second bundle within the second cluster (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

8. Referring to claim 4, Batten has taught architecting data from the first cluster to a first register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

9. Referring to claim 5, Batten has taught committing architected state from the second cluster to the first register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

10. Referring to claim 6, Batten has taught architecting data from the second cluster to a second register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

11. Referring to claim 7, Batten has taught fetching the first bundle comprising decoding instructions into the first bundle of the singly-threaded instructions (Batten column 11, lines 1-15 and Figure 12).

12. Referring to claim 8, Batten has taught fetching the second bundle comprising decoding instructions into the second bundle of the singly-threaded instructions (Batten column 11, lines 1-15 and Figure 12).

13. Referring to claim 9, Batten has taught

a. Fetching a third bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the third bundle to the first and second clusters of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

c. Bypassing data between the clusters, as needed, to facilitate processing of the third bundle through the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6).

14. Referring to claim 10, Batten has taught utilizing a latch to couple the data between the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6). In regards to Batten, the file replication technique and cooperative interconnection technique

requires the data to be moved from private cluster registers to global registers before the destination cluster can read the data and move/write the data into its private registers. The intermediate, global register is a type of latch. Please see FOLDOC's definitions of "latch" and "register."

15. Referring to claim 11, Batten has taught selecting a configuration bit prior to the steps of fetching the third bundle, distributing the third bundle, and bypassing (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

16. Referring to claim 12, Batten has taught a method for processing bundled instructions through execution units of a processor, comprising the steps of:

a. Fetching a first bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the first bundle to two or more clusters of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

c. Bypassing data between the clusters, as needed, to facilitate processing of the first bundle through the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6).

17. Referring to claim 13. Batten has taught

a. Fetching a second bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the second bundle to one of the clusters for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

c. Fetching a third bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

d. Distributing the third bundle to another one of the clusters units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

18. Referring to claim 13, Batten has taught selecting a configuration bit prior to the steps of fetching the second bundle, distributing the second bundle, fetching a third bundle and distributing the third bundle (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

19. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being taught by Murata et al., U.S. Patent Number 5,729,761 (herein referred to as Murata)

20. Referring to claim 15, Murata has taught in a processor architecture of the type having two or more clusters of execution units for processing instructions (Murata column 1, line 54 to column 2, line 19; column 2, line 56 to column 3, line 17; and Figure 1), the improvement comprising a thread decoder for grouping instructions into singly threaded bundles and for

distributing the bundles to the clusters according to either a wide mode or throughput mode of operation (Murata column 1, line 54 to column 2, line 19; column 3, lines 44-55; column 4, lines 60 to column 4, line 6; column 4, lines 15-26 and 33-52; column 9, lines 6-26 and 49-62; Figure 3; Figure 4; Figure 5; Figure 10; Figure 11; and Figure 12).

21. Referring to claim 16, Murata has taught wherein each cluster comprises a core and register file (Murata column 1, line 54 to column 2, line 19; column 2, line 56 to column 3, line 17; and Figure 1).

22. Referring to claim 17, Murata has taught wherein the thread decoder distributes bundles of singly-threaded instructions through a multiple of clusters in the wide mode of operation, and wherein the thread decoder distributes bundles of singly-threaded instructions through one of the clusters in the throughput mode of operation (Murata column 1, line 54 to column 2, line 19; column 3, lines 44-55; column 4, lines 60 to column 4, line 6; column 4, lines 15-26 and 33-52; column 9, lines 6-26 and 49-62; Figure 3; Figure 4; Figure 5; Figure 10; Figure 11; and Figure 12).

Response to Arguments

23. Examiner withdraws the drawing objections in favor of the amended drawings.

24. Examiner withdraws the specification objections in favor of the amended specification.

25. Examiner withdraws the claim objections and 35 U.S.C. §112, second paragraph rejection in favor of the amended claims.

26. Applicant's arguments filed 04 April 2005 have been fully considered but they are not persuasive.

27. Applicant argues in essence on page 8

> ...Batten does not disclose, or even suggest, two modes of operation, the bundling of instructions, or the processing of instructions from one thread through one cluster. In fact, Batten does not disclose any specific method of processing instructions at all, let alone bundling instructions in association with threads.

28. This has not been found persuasive. Claim 1 has "singly-threaded instructions" which, in the broadest reasonable interpretation, are instructions from a single thread, i.e. instructions from the same program. Batten's device fetches instructions from a program in memory (Batten column 11, lines 1-15 and Figure 12). Therefore, the instructions are "singly-threaded instructions" since the instructions are from the same program. Also, claim 1, for example, does not require that there be two modes of operation or the processing of instructions from one thread through one cluster. There is no apparent language in the claim restricting the device to two modes or one cluster for one thread. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., two modes of operation and one thread for one cluster) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

29. Applicant's argue in essence on pages 9-11

> As noted, Batten does not disclose or suggest bundling instructions, nor fetching singly-threaded instructions as required by step a). Batten also does not disclose or suggest distributing bundled instructions to a specific cluster, as required by step b). Batten further does not disclose fetching a second bundle of

singly-threaded instructions, as required by step c). And Batten does not disclose executing singly-threaded instructions on a specific cluster, as required by step d).

Notably, Batten makes no distinction between processing of threads and does not teach, suggest, or disclose the bundling of instructions. Batten, therefore, cannot anticipate claim 1...

30. This has not been found persuasive. Batten discloses in column 7, lines 12-20 that processor that are in accordance with the invention include very long instruction word (VLIW) processors and multi-issue processors. In these types of processors with the multiple execution clusters of Batten's Figure 12, instruction bundles, i.e. more than one instruction, are executed. For example, in a VLIW processor, the VLIW is actually multiple instructions in one, i.e. an instruction bundle. For more information about VLIW please see InstantWeb's "Online Computing Dictionary". In a multi-issue processor, multiple instructions are issued at the same time to different execution clusters/units. For more information about multi-issue processors, also known as superscalar processors, please see InstantWeb's "Online Computing Dictionary". The simultaneous issues of multiple instructions, i.e. issue of instruction bundles, is supported in Batten in column 1, lines 28-32 which states "A significant problem with wide-issue load-store micro-processors is port pressure on the register file, i.e., the register file must support a large number of simultaneous accesses..." The only time a register file needs to support "a large number of simultaneous accesses" is when several instructions execution units, which are controlled by individual instructions, try to access the data held within the register file simultaneously. Therefore, Batten has taught the bundling of instructions. In regards to the teaching of processing of treads, none of the claims recite any language relating to having

multiple threads, as insinuated in the arguments. There is only language regarding having one thread, i.e. "singly threaded". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., multiple threads) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

31. Applicant argues in essence on pages 11-12

> Murata does not disclose or suggest a thread decoder for grouping instructions into singly-threaded bundles and for distributing the bundles to the clusters according to either a wide mode or a throughput mode of operation...

32. This has not been found persuasive. There is nothing in the claim to further define "wide mode" and "throughput mode" other than the common definition of the terms. In Murata, the "wide mode" is when the instructions are distributed across all clusters for execution, since the instructions are used processor wide, i.e. across all clusters. The "throughput mode" is when the instructions are only executed by one cluster, since the instructions are only executed through one processor.

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
17 June 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100